What is claimed is:

1. An analog front end circuit converting an analog signal outputted by an image sensor into a digital signal, the analog signal comprising a first voltage level signal and a first reference signal, the analog front end circuit comprising:

a sample and hold circuit comprising:

a variable gain amplifier circuit comprising a first input end, a second input end, and at least one output end, the first input end being used for receiving the first voltage level signal, the second input end being used for receiving the first reference signal, the output end being used for outputting at least an amplified signal,

a first sample switch in the front end of the first input end,

a second sample switch in the front end of the second input end, and

a hold switch connected between the first input end and the second input end,

wherein while the first sample switch is at a first conductive state, the first input end receives the first voltage level signal, while the second sample switch is at the first conductive state, the second input end receives the first reference signal, and while the hold switch is at a second conductive state, the output end outputs the amplified signal; and

an analog to digital converter device for receiving the amplified signal and converting the amplified signal into the digital signal.

2. The analog front end circuit of claim 1, wherein the first sample switch and the second sample switch are both controlled by a sample pulse signal.

3. The analog front end circuit of claim 1, wherein the hold switch is controlled by a hold pulse signal.

4. The analog front end circuit of claim 1, wherein the sample and hold circuits further comprise a first buffer for receiving a charged-coupled device signal and shifting a second voltage level signal of the charged-coupled device signal to the first voltage level signal.

5. The analog front end circuit of claim 4, wherein the first buffer comprises:

a first P channel metal oxide semiconductor having a first source, a first gate, and a first drain;

a second P channel metal oxide semiconductor having a second source, a second gate, and a second drain; and

an output end of the first buffer;

wherein the first source is connected to a power supply, the second drain is grounded, a first bias voltage is inputted to the first gate, the charged-coupled device signal is inputted to the second gate, and the first drain and the second source are both connected to the output end of the first buffer.

6. The analog front end circuit of claim 1, wherein the sample and hold circuit further comprises a second buffer for receiving a control signal to generate the first reference signal.

7. The analog front end circuit of claim 6, wherein the second buffer comprises:

a third P channel metal oxide semiconductor having a third source, a third gate, and a third drain;

a fourth P channel metal oxide semiconductor having a fourth source, a fourth gate, and a fourth drain; and

an output end of the second buffer;

wherein the third source is connected to the power supply, the fourth drain is grounded, a third bias voltage is inputted to the third gate, the first reference

signal is inputted to the fourth gate, and the third drain and the fourth source are both connected to the output end of the second buffer.

8. The analog front end circuit of claim 1, wherein the variable gain amplifier circuit further comprises:

an operational amplifier comprising a first differential input end, a second differential input end, a first differential output end, and a second differential output end;

a first capacitor connected to the first input end and the first differential input end, wherein the capacitance value of the first capacitor is C1;

a second capacitor connected to the second input end and the second differential input end, wherein the capacitance value of the second capacitor is C2;

a third capacitor and a third sample switch, individually connected to the first differential input end and the first differential output end, wherein the capacitance value of the third capacitor is C3; and

a fourth capacitor and a fourth sample switch, individually connected to the second differential input end and the second differential output end, wherein the capacitance value of the fourth capacitor is C4.

9. The analog front end circuit of claim 8, wherein the amplified signal comprises a first amplified signal and a second amplified signal, the difference between the first amplified signal and the second amplified signal is the product of the difference between the first voltage level signal and the first reference signal and a gain value of the variable gain amplifier circuit, and the gain value is calculated by the following equation:

$$G=C1/C3;\ C1:C3=C2:C4$$

10. The analog front end circuit of claim 9, wherein the output end comprises the first differential output end and the second differential output end, the first differential output end is used for outputting the first amplified signal, and the second differential output end is used for outputting the second amplified signal.

11. The analog front end circuit of claim 1, wherein the analog to digital converter device further comprises:

an analog adder for receiving a DC signal and the amplified signal to output a converted voltage signal; and

an analog to digital converter for receiving the converted voltage signal and converting the converted voltage signal into the digital signal.

12. An analog front end signal process method converting an analog signal outputted by an image sensor to a digital signal, the analog signal comprising a first voltage level signal and a first reference signal, the method comprising the following steps:

(a) receiving the first voltage level signal by a first input end of a variable gain amplifier circuit when a first sample switch in the front end of the first input end is set at a first conductive state;

(b) receiving the first reference signal by a second input end of the variable gain amplifier circuit when a second sample switch in the front end of the second input end is set at the first conductive state;

(c) outputting at least one amplified signal via an output end of the variable gain amplifier circuit when a hold switch connected between the first input end and the second input end is at a second conductive state; and

(d) converting the amplified signal into the digital signal.

13. The method of claim 12, wherein the first sample switch and the second sample switch are both controlled by a sample pulse signal.

14. The method of claim 12, wherein the hold switch is controlled by a hold pulse signal.

15. The method of claim 12, wherein the first voltage level signal is generated by a first buffer, and the first buffer is used for receiving a charged-coupled device signal and shifting a second voltage level signal of the charged-coupled device signal to the first voltage level signal.

16. The method of claim 15, wherein the first buffer comprises:

a first P channel metal oxide semiconductor having a first source, a first gate, and a first drain;

a second P channel metal oxide semiconductor having a second source, a second gate, and a second drain; and

an output end of the first buffer;

wherein the first source is connected to a power supply, the second drain is grounded, a first bias voltage is inputted to the first gate, the charged-coupled device signal is inputted to the second gate, and the first drain and the second source are both connected to the output end of the first buffer.

17. The method of claim 12, wherein the first reference signal is generated by a second buffer, and the second buffer is used for receiving a control signal to generate the first reference signal.

18. The method of claim 17, wherein the second buffer comprises:

a third P channel metal oxide semiconductor having a third source, a third gate, and a third drain;

a fourth P channel metal oxide semiconductor having a fourth source, a fourth gate, and a fourth drain; and

an output end of the second buffer;

wherein the third source is connected to the power supply, the fourth drain is grounded, a third bias voltage is inputted to the third gate, the first reference signal is inputted to the fourth gate, and the third drain and the fourth source are both connected to the output end of the second buffer.

19. The method of claim 12, wherein the variable gain amplifier circuit further comprises:

an operational amplifier comprising a first differential input end, a second differential input end, a first differential output end, and a second differential output end;

a first capacitor connected to the first input end and the first differential input end, wherein the capacitance value of the first capacitor is C1;

a second capacitor connected to the second input end and the second differential input end, wherein the capacitance value of the second capacitor is C2;

a third capacitor and a third sample switch, individually connected to the first differential input end and the first differential output end, wherein the capacitance value of the third capacitor is C3; and

a fourth capacitor and a fourth sample switch, individually connected to the second differential input end and the second differential output end, wherein the capacitance value of the fourth capacitor is C4.

20. The method of claim 19,wherein the amplified signal comprises a first amplified signal and a second amplified signal, the difference between the first amplified signal and the second amplified signal is the product of the difference between the first voltage level signal and the first reference signal and a gain value of the variable gain amplifier circuit, and the gain value is calculated by the following

equation:

$$G=C1/C3 \; ; \; C1:C3=C2:C4$$

21. The method of claim 20, wherein the output end comprises the first differential output end and the second differential output end, the first differential output end is used for outputting the first amplified signal, and the second differential output end is used for outputting the second amplified signal.

22. The method of claim 12, wherein the step (d) further comprises the following steps:

(d1) adding the amplified signal and a DC signal to output a converted voltage signal; and

(d2) converting the converted voltage signal into the digital signal.